IN THE SPECIFICATION:

Please amend paragraph [0001] as follows:

[0001] This application is a continuation of U.S. Patent Application Serial No. 10/150,902, filed May 17, 2002, ~~pending,~~ now U.S. Patent 6,975,035, issued December 13, 2005, which application is related to U.S. Patent Application Serial No. 09/944,465, filed August 30, 2001, now U.S. Patent 6,756,251, issued June 29, 2004, and entitled MICROELECTRONIC DEVICES AND METHODS OF MANUFACTURE, and to the following U.S. Patent Applications filed on ~~even date herewith:~~ May 17, 2002: Serial No. 10/150,893, entitled INTERPOSER CONFIGURED TO REDUCE THE PROFILES OF SEMICONDUCTOR DEVICE ASSEMBLIES AND PACKAGES INCLUDING THE SAME AND METHODS; Serial No. 10/150,892, entitled METHOD AND APPARATUS FOR FLIP-CHIP PACKAGING PROVIDING TESTING CAPABILITY; Serial No. 10/150,516, entitled SEMICONDUCTOR DIE PACKAGES WITH RECESSED INTERCONNECTING STRUCTURES AND METHODS FOR ASSEMBLING THE SAME; Serial No. 10/150,653, entitled FLIP CHIP PACKAGING USING RECESSED INTERPOSER TERMINALS; and Serial No. 10/150,901, entitled METHODS FOR ASSEMBLY AND PACKAGING OF FLIP CHIP CONFIGURED DICE WITH INTERPOSER.

Please amend paragraph [0008] as follows:

[0008] Further, flip chip packages for a bumped semiconductor die employing an interposer may be undesirably thick due to the combined height of the die and interposer. This is due to the use in conventional packaging techniques of relatively costly interposers comprising dual conductive layers having a dielectric member sandwiched therebetween, the bumped semiconductor die resting on and connected to traces of the conductive layer on one side of the interposer and electrically connected to traces of the conductive layer on the opposing side, conductive vias extending therebetween. Finally, underfilling a flip chip-attached semiconductor die to a carrier substrate with dielectric filler material can be a lengthy and often unreliable

process, and the presence of the underfill makes reworking of defective assemblies ~~difficult~~ difficult, if not impossible.

Please amend paragraph [0010] as follows:

[0010] For example, United States Patent ~~No.~~ 5,710,071 to Beddingfield et al. discloses a fairly typical flip chip attachment of a semiconductor die to a substrate and a method of underfilling a gap between the semiconductor die and substrate. In particular, the semiconductor die is attached face down to the substrate, wherein conductive bumps on the die are directly bonded to bond pads on the upper surface of the substrate, which provides the gap between the die and substrate. The underfill material flows through the gap between the semiconductor die and the substrate via capillary action toward an aperture in the substrate, thereby expelling air in the gap through the aperture in the substrate in an effort to minimize voids in the underfill material. However, such an underfilling method still is unnecessarily time consuming due to having to underfill the entire semiconductor die. Further, the flip chip attachment technique disclosed in United States Patent ~~No.~~ 5,710,071 exhibits difficulties in aligning the conductive bumps with the bond pads on the substrate and requires the expense of having a third metal reroute in the substrate.

Please amend paragraph [0034] as follows:

[0034] FIGS. 8A - 8D illustrate a third method of mounting a semiconductor die face down to an interposer substrate in a flip ~~chip~~ chip-type semiconductor device assembly according to the present invention;

Please amend paragraph [0058] as follows:

[0058] The interposer substrate 110 may be formed from any known substrate material and is preferably formed of, by way of example, a flexible laminated polymer or polyimide layer, such as UPILEX®, produced by Ube Industries, Ltd., or any other polymer-type layer. The interposer substrate 110 may also be made of a bismaleimide triazine (BT) resin, ~~FR-4, FR-5~~

FR4, FR5 laminates or any type of substantially nonflexible material, such as a ceramic or epoxy resin.

Please amend paragraph **[0061]** as follows:

[0061] It will be observed in FIG. 1 that conductive traces 124 extend over recesses 120 and may optionally extend therebeyond, if desired, for enhanced adhesion of conductive traces 124 to dielectric substrate member 111. Conductive pads or terminals 122 may completely cover the bottoms of recesses 120 or, as depicted in FIG. 1, may be narrower than recesses 120 at the bottoms thereof so that gaps 121 are defined on one or both sides of conductive pads or terminals 122. As implied above, the conductive ~~traces,~~ traces 124, which may, for example, comprise copper or a copper alloy, may be adhered to the dielectric substrate member of UPILEX®, BT resin, ~~FR-4 or, FR-5~~ FR4 or FR5 laminate material, or other substrate materials, using adhesives as known in the art. In some instances, the material of the conductive traces may be adhesively laminated to the dielectric substrate member in the form of a conductive sheet, the traces then being subtractively formed from the conductive sheet, as by etching.

Please amend paragraph **[0062]** as follows:

[0062] Further, interposer substrate 110 may also include an opening 130 (shown in broken lines) formed thereacross, the opening 130 substantially extending along a longitudinal extent of the centrally aligned, single-row configuration of the multiple recesses 120 from one end of interposer substrate 110 to the other. Opening 130 may be formed wholly in the material of dielectric substrate member 111, or may, as shown by the broken lead line from reference numeral 130 in FIG. 2 and the broken lead line from reference numeral 130 in FIG. 3, be formed in solder mask 118. Of course, opening 130 may be formed partially in dielectric substrate member 111 and partially in solder mask 118, as desired. Opening 130 may be formed to align along any employed recess configuration, *i.e.*, I-shape or peripheral. To better illustrate opening 130, FIG. 2 depicts a cross-sectional view taken along ~~lines~~ line 2-2 in FIG. 1. As illustrated, opening 130 includes multiple segments 132, each segment 132 extending between

separate individual recesses 120 of the multiple recesses 120. Further, each segment 132 as shown extends along the axis of opening 130 to a side portion of each of the recesses 120; however, the segments 132 may extend and be positioned from the opening 130 to the recesses 120 in any suitable manner. For example, and as depicted in FIG. 1A, opening 130 may comprise a slot laterally offset from recesses 120, which are themselves defined between fingers 111f of flexible dielectric substrate member 111 which terminate at opening 130. As shown, conductive traces 124 extend across opening 130, and solder mask 118 covers the end portions thereof flanking opening 130 and providing an enhanced depth and width to opening 130 for underfilling purposes.

Please amend paragraph **[0063]** as follows:

[0063] To further illustrate opening 130, FIG. 3 is a cross-sectional view taken along ~~lines~~ line 3-3 of FIG. 1. FIG. 3 depicts opening 130 extending directly into the recesses 120, i.e., into the plane of the drawing sheet. Such opening 130 is shown as having a lateral width smaller than the recesses 120; however, the opening may be sized substantially equal to, or larger than, the lateral width of the recesses 120. FIG. 3 also depicts conductive pads or terminals 122 at the bottom of each of the recesses 120 interconnected through conductive traces 124 with conductive pads 126 exposed at the second surface 114 of the interposer substrate 110 through solder mask 118.

Please amend paragraph **[0066]** as follows:

[0066] FIG. 4B depicts dielectric substrate member 111 with one of the recesses 120 formed therein. Such recesses 120 may be formed by patterning, utilizing a chemical wet etch or dry etch, mechanical drilling or punching, laser ablation, or any method known in the art and suitable for use with the type of material employed for the dielectric substrate member 111. The recesses 120 are preferably formed to expose portions of one of the conductive traces 124, such as conductive pads or terminals 122. At a bottom of each recess 120 and, for example, at the location of each conductive pad or terminal 122, additional conductive material may be placed,

such as gold or eutectic tin/lead solder, the material selected being compatible with the conductive material of the conductive traces 124 and with the bumps of a semiconductor die to be mated with interposer substrate 110. FIG. 4C illustrates that the walls of the recesses 120 may include a conductive layer 123 formed thereon, for example, by electroless plating; however, such plating is not required for practice of the present invention. Further and as shown in FIGS. 4B and 4C, ~~recesses~~ recesses 120 may be formed with large mouths which taper to a smaller bottom. Such tapering may be easily effected using isotropic etching techniques as known in the art.

Please amend paragraph **[0067]** as follows:

[0067] FIGS. 5A through 5D depict a process similar to that depicted and described in FIGS. 4A - 4C of forming recesses 120 in the first surface 112 of interposer substrate 110, with the addition of another layer, namely, a second conductive layer 125, as shown in FIG. 5A. Such second conductive layer 125 is preferably a copper or copper alloy layer, but may be any suitable electrically conductive material, and may be patterned with traces, depending on the needs and requirements of the particular semiconductor die to which the interposer substrate 110 is attached. FIG. 5B depicts second conductive layer 125 patterned to expose portions of dielectric substrate member 111 where the recesses 120 are to be formed and substantially etched back from the intended lateral boundaries of the recess ~~mouths~~ mouths. As shown in FIG. 5C, a recess 120 is then formed in the exposed portions of dielectric substrate member 111 by a chemical wet etch or dry etch, mechanical drilling or ~~punching~~ punching, or laser ablation; however, the recess 120 may be formed utilizing any method known in the art and suitable with the type of material employed for the interposer substrate 110. The recesses 120 are preferably formed to expose conductive pads or terminals 122 of the conductive traces 124, after which additional conductive material may be placed over the exposed portion of the conductive pads or terminals 122. As before, a conductive layer 123 may be formed by electroless plating on the walls of the recesses 120 so that such conductive layer 123 contacts a portion of the conductive pads or terminals 122 of the exposed conductive traces 124, as depicted in FIG. 5D. As shown in

FIGS. 5A through 5D in solid lines, solder mask 118 may provide full coverage over the bottoms of conductive traces 124 or~~, as shown in broken lines,~~ may include an aperture or apertures therethrough, for example, to provide an opening 130, as shown in broken lines, to expose the undersides of conductive traces 124 at the locations of recesses 120 or otherwise, as desired, for enhanced underfill access. If a wet solder mask 118 is employed, recesses 120 in dielectric substrate member 111 are plugged with a removable material before solder mask application; if a dry (film) solder mask 118 is employed, it may merely be laminated to dielectric substrate member 111.

Please amend paragraph **[0068]** as follows:

[0068] FIGS. 6A - 6B depict simplified cross-sectional views of a first method of mounting and bonding interposer substrate 110 to a semiconductor die 150 in a flip chip-type semiconductor device assembly 160. FIG. 6A illustrates the first surface 112 of interposer substrate 110 aligned and facing the semiconductor die 150 prior to the assembly thereof. Semiconductor die 150 includes an active surface 152 and a back side or surface 154, wherein the active surface 152 includes a plurality of bond pads 158 bearing electrically conductive bumps 156 thereon. Such conductive bumps 156 and bond pads 158 of semiconductor die 150 are of a preselected configuration, wherein the recesses 120 in interposer substrate 110 are sized and configured to correspond with the configuration of the bond pads 158 and conductive bumps 156 of semiconductor die 150 so that the respective configurations or patterns of recesses 120 and conductive bumps 156 are substantially mirror images of each other. As shown, solder mask 118 may have an opening 130 defined therethrough or, alternatively, full solder ~~mask~~ mask 118 coverage may be provided across the bottoms of conductive traces 124, including the locations of recesses 120 as previously described with respect to FIGS. 5A through 5D.

Please amend paragraph [0070] as follows:

[0070] FIG. 6B depicts interposer substrate 110 mounted to semiconductor die 150 to form flip chip semiconductor device assembly 160, wherein such assembly 160 provides that each of the conductive bumps 156 is substantially inserted in a corresponding recess 120 of interposer substrate 110 and engages with the conductive pad or terminal 122 at the bottom of each of the recesses 120. Such flip chip semiconductor device assembly 160 may be initially attached by the adhesive element 116 carried on the first surface 112 of the interposer substrate 110. The conductive bumps 156 on the semiconductor die 150 may then be bonded to the conductive pads or terminals 122 in the recesses 120 of interposer substrate 110 by, for example, reflowing the conductive bumps 156 (in the case of solder bumps) or curing the conductive bumps 156 (in the case of conductive or conductor-filled polymer bumps) as known in the art. Other methods of bonding known in the art may be utilized, such as ultrasonic or thermal compression.

Please amend paragraph [0071] as follows:

[0071] FIGS. 7A - 7B depict simplified cross-sectional views of a second method of mounting and bonding interposer substrate 110 to a semiconductor die 150 in a flip chip semiconductor device assembly 160. FIG. 7A illustrates the first surface 112 of interposer substrate 110 aligned with and facing the semiconductor die 150 prior to the assembly thereof. FIG. 7A is similar to FIG. 6A in substantially every respect, except the conductive bumps 156 on the semiconductor die 150 carry a conductive paste 182 thereon. Such conductive paste 182 may be provided on the conductive bumps 156 by dipping the conductive bumps 156 into a pool of conductive paste 182 or by depositing, dispensing or otherwise transferring the conductive paste 182 to the conductive bumps 156. The conductive paste 182 may include, but is not limited to, eutectic solder, conductive epoxy, or any nonsolid conductive material known in the art. As shown, solder mask 118 may have an opening 130 defined therethrough or, alternatively, full solder ~~mask~~ mask 118 coverage may be provided across the bottoms of conductive

traces 124, including the locations of recesses 120 as previously described with respect to FIGS. 5A through 5D.

Please amend paragraph **[0072]** as follows:

[0072] As depicted in FIG. 7B, the interposer substrate 110 is mounted to semiconductor die 150 to form flip chip semiconductor device assembly 160, wherein each of the conductive bumps 156 is substantially inserted into a corresponding recess 120 of interposer substrate 110 with the conductive paste 182 engaging with the conductive pad or terminal 122 in each of the recesses 120. With this arrangement, the conductive paste 182 provides contact with the conductive pads or terminals 122 even if some of the conductive bumps 156 are inconsistent in height, *i.e.*, their free ends are noncoplanar. Such conductive bumps 156 having the conductive ~~paste~~ paste 182 provided thereon may then be bonded to the conductive pads or terminals 122 in the recesses 120 of interposer substrate 110 as previously described in association with FIGS. 6A and 6B.

Please amend paragraph **[0074]** as follows:

[0074] With the conductive paste 182 in the recesses 120, FIG. 8C depicts the interposer substrate 110 mounted to semiconductor die 150 to form semiconductor device assembly 160, wherein each of the conductive bumps 156 is substantially inserted into the conductive paste 182 in the corresponding recesses 120 of interposer substrate 110. As previously described in FIG. 7B, the conductive paste 182 provides electrical and mechanical interconnection between the conductive pads or terminals 122 or trace ends and the conductive bumps 156 even if some of the conductive bumps 156 are inconsistent in height, *i.e.*, their free ends are noncoplanar. The semiconductor die 150 may then be bonded with the interposer substrate 110 as previously described in association with FIGS. 6A and 6B. It will be understood, as noted above, that stencil 186 may not be required if the mass of conductive paste 182 is disposed and spread into recesses 120 prior to disposition of an adhesive element 116 over first surface 112. Moreover, it will be understood that conductive paste 182, if

eutectic solder, may be disposed in recesses 120 and then reflowed and solidified prior to attachment of semiconductor die 150 to interposer substrate 110 using a second reflow to provide an indefinite shelf life for interposer substrate 110. Alternatively, semiconductor die 150 may be aligned with interposer substrate 110 after conductive ~~paste~~ paste 182 disposition and a single reflow employed. FIG. 8D is an enlarged view of a single conductive bump 156 carried by a semiconductor die 150 in initial contact with a mass of conductive paste 182 disposed in a recess 120 in dielectric substrate member 111 of interposer substrate 110 over conductive pad or terminal 122 of a conductive trace 124.

Please amend paragraph **[0076]** as follows:

[0076] FIGS. 9A - 9B depict simplified cross-sectional views of a variant of the above-described third method comprising a fourth method of preparing, mounting and bonding interposer substrate 110 to a semiconductor die 150 in a flip chip semiconductor device assembly 160. Such variant is similar to the third method as described in FIGS. 8A - 8D of providing conductive ~~paste~~ paste 182 in each of the recesses 120, except the conductive bumps 156 are initially unattached to the bond pads 158 of the semiconductor die 150. As depicted in FIG. 9A, the conductive bumps 156 in the form of balls, such as metal balls, are embedded into the conductive paste 182, which was previously spread into the recesses 120 of the interposer substrate 110. The bond pads 158 in the semiconductor die 150 are aligned with the conductive bumps 156 in the recesses 120 in the interposer substrate 110 and then mounted thereto, as depicted in FIGS. 9A - 9B. The conductive paste 182 may comprise a solder wettable to both bond pads 158 and conductive pads or terminals 122 or a conductive or conductor-filled adhesive. It will also be understood and appreciated that conductive bumps 156 may themselves comprise solder, such as a PbSn solder, and conductive paste 182 may be eliminated, or may also ~~comprising~~ comprise a compatible solder.

Please amend paragraph [0077] as follows:

[0077] As a further alternative and as previously described with respect to FIGS. 8A and 8B, a conductive bump ~~156~~ 156, to be used in lieu of a conductive bump 156 carried by semiconductor die ~~150~~ 150, may be formed in each of recesses 120 through plating of conductive pads or terminals 122 with a conductive material such as a suitable metal.

Please amend paragraph [0078] as follows:

[0078] It will be well appreciated by one of ordinary skill in the art that, since the conductive bumps 156 are bonded within the recesses 120 of the interposer substrate 110 itself, the height of the flip chip semiconductor device assembly 160 is minimized. Therefore, conductive bumps 156 may be formed larger in size than those of conventional flip chip assemblies without increasing, or even while decreasing, the height of the flip chip semiconductor device assembly 160, resulting in the increase in electrical and mechanical reliability and performance of the interconnections between the interposer substrate 110 and the semiconductor die 150. Further, the recesses 120 in the interposer substrate 110 provide an inherent alignment aspect absent in a conventional flip chip semiconductor device assembly because the conductive bumps 156 easily slide into their respective corresponding recesses 120 to ensure proper alignment and proper attachment thereof. In addition, the adhesive element 116 on the first surface 112 of the interposer substrate 110 as well as the conductive paste 182 in the recesses 120 may act as a height controller for reliable attachment of the semiconductor die 150 to the interposer substrate 110, wherein the adhesive element 116 and/or the conductive paste 182 may be used to compensate for any irregularities due to varied conductive ~~bump~~ bump 156 sizes, recess depths and planarity variation in the surfaces of the interposer substrate 110 and semiconductor die 150.

Please amend paragraph [0079] as follows:

[0079] As shown in FIG. 10, a dielectric filler material 166 (commonly termed an "underfill" material) may be optionally applied through opening 130. The method employed to

apply the dielectric filler material 166 preferably involves dispensing under pressure from dispenser head 164, but may include any method known in the art, such as gravity and vacuum injecting. In this manner, the dielectric filler material 166 may be applied into the opening 130, move as a flow front through the multiple segments 132 (see FIG. 1) and into each of the recesses 120 to fill a space around the conductive bumps 156, bond pads 158 and conductive pads or terminals 122. The dielectric filler material 166 may be self-curing through a chemical reaction, or a cure accelerated by heat, ultraviolet light or other radiation, or other suitable means may be used in order to form at least a semisolid mass in the recesses 120. Such dielectric filler material 166 provides enhanced securement of the components of flip chip semiconductor device assembly 160 as well as precluding shorting between conductive elements and protecting the conductive elements from environmental concerns, such as moisture. As such, compared to the conventional underfilling of the entire semiconductor ~~die,~~ die 150, the semiconductor device assembly 160 of the present invention requires less time since the dielectric filler material 166 may only be directed to fill the recesses 120 or, rather, any leftover space within the recesses 120 proximate the interconnections, *i.e.*, conductive bumps 156.

Please amend paragraph **[0080]** as follows:

[0080] Turning back to the third and fourth methods depicted in FIGS. 8A - 8D and 9A - 9B, the interposer substrate 110 described for use in such methods may not include an opening for applying dielectric filler material 166 to the recesses 120 because the recesses 120 are substantially filled with conductive paste 182. Therefore, it is contemplated that applying dielectric filler material 166 through an opening 130 in the interposer substrate 110 described in the third and fourth methods may not be necessary.

Please amend paragraph **[0082]** as follows:

[0082] FIG. 11 also depicts flip chip semiconductor device assembly 160 attached to another carrier substrate 170, such as a printed circuit board or ~~mother board.~~ motherboard. The carrier substrate 170 includes a substrate upper surface 172 and a substrate lower surface 174,

upper surface 172 bearing substrate terminal pads 176 arranged to correspond and attach with conductive balls 162 on the second surface 114 of interposer substrate 110. As such, the flip chip semiconductor device assembly 160 may be mechanically and electrically connected to carrier substrate 170 by reflowing the conductive (solder) balls 162 to the substrate terminal pads 176. A dielectric filler material (not shown) as known in the art may then be applied between the flip chip semiconductor device assembly 160 and the carrier substrate 170 for securing and protecting the interconnections, *i.e.*, conductive balls 162, therebetween.

Please amend paragraph **[0088]** as follows:

[0088] As in the first embodiment, the semiconductor die 650 in the flip chip semiconductor device assembly 660 of the second embodiment may then be either fully encapsulated or partially encapsulated by encapsulation apparatus 178 with an encapsulation material 168 as depicted in FIG. 17. In the case of partially encapsulating the semiconductor die 650, encapsulation material 168 may be dispensed by dispenser head 164 about the periphery of the semiconductor die 650 so that the back side or surface 654 of the die is left exposed. In the case of fully encapsulating the die, encapsulation material 168 may be applied to the back side or surface 654 of the semiconductor die 650 (which may include at the wafer level) prior to dispensing encapsulation material 168 about the periphery of the semiconductor die 650 in order to facilitate fully encapsulating the semiconductor die 650.

Please amend paragraph **[0089]** as follows:

[0089] FIG. 17 also depicts semiconductor device assembly 660 attached to another substrate 170, such as a printed circuit board or ~~mother board.~~ motherboard. The substrate 170 includes a substrate upper surface 172 and a substrate lower surface 174 with substrate terminal pads 176 made to correspond and attach with conductive balls 662, such as solder balls, on the second surface 614 of interposer substrate 610. Conductive balls 662, if solder, may be formed by placement of solder paste on conductive pads 626 followed by reflow, preformed and secured to conductive pads 626, applied to substrate terminal pads 176, or otherwise as known in the art.

As such, the semiconductor device assembly 660 may be bonded to substrate 170 by reflowing the conductive balls 662 to the substrate terminal pads 176. A dielectric filler material (not shown) may then be applied between the semiconductor device assembly 660 and the substrate 170 for securing and protecting the interconnections, *i.e.*, conductive balls 662, therebetween.

Please amend paragraph **[0092]** as follows:

[0092] FIG. 22 depicts the channel 740 having a channel opening 744 at a side periphery of the semiconductor assembly 760, through which dielectric filler material 166 may be introduced. Such dielectric filler material 166 may be dispensed from dispenser head 164 proximate the channel opening 744, wherein dielectric filler material 166 may flow and fill in spaces around the conductive bumps 756 in the recesses 720. Such process may be employed with the semiconductor assembly 760 horizontal, vertical, or at any angle which may promote the dielectric filler material 166 to fill the recesses 720. The dielectric filler material 166 introduction may also be enhanced by a vacuum or suction means to optimize the time it takes to fill in the recesses 720. Further, if conductive pads or terminals 722 cover the bottoms of recesses 720, each conductive pad or terminal 722 may be provided with a hole therethrough through which air may be expelled by the flow front **F** of dielectric filler material 166 or to which a vacuum may be applied. As in the previous embodiments, semiconductor die 750 may be fully encapsulated, including back side or surface 754, with encapsulation apparatus 178 and dispenser head 164 or partially encapsulated with dispenser head 164, as depicted in FIG. 23.

Please amend paragraph **[0093]** as follows:

[0093] FIG. 23 also depicts semiconductor assembly 760 attached to another substrate 170, such as a printed circuit board or ~~mother board.~~ motherboard. The substrate 170 includes a substrate upper surface 172 and a substrate lower surface 174 with substrate terminal pads 176 made to correspond and attach with conductive balls 762, such as solder balls, on the second surface 714 of interposer substrate 710. As such, the semiconductor assembly 760 may

be bonded to substrate 170 by reflowing the conductive balls 762 to the substrate terminal pads 176. A filler material (not shown) may then be applied between the semiconductor assembly 760 and the substrate 170 for securing and protecting the interconnections, *i.e.*, conductive balls 762, therebetween.

Please amend paragraph **[0096]** as follows:

[0096] Also at the wafer level and as previously described in association with FIGS. 6A - 6B, 7A - 7B, 8A - 8D, 9A - 9B, the conductive bumps 256 may be bonded to the conductive pads or terminals in the recesses 220 to, therefore, mechanically bond and electrically connect the semiconductor wafer 250 to the wafer scale interposer substrate 210. In addition, dielectric filler ~~material~~ material 166 may be applied through the openings 230 and conductive balls 262 may be provided on the bond posts on the second surface 214 of the interposer substrate 210, either prior to dicing the wafer scale assembly 260, or subsequent thereto.

Please amend paragraph **[0099]** as follows:

[0099] FIG. 27 depicts a cross-sectional view of a semiconductor assembly 460 including a semiconductor die 450 mounted face down to an interposer substrate 410 having a peripheral recess configuration and an alternative method of applying dielectric filler material 166 to the semiconductor assembly 460. In particular, dielectric filler material 166 may be applied by dispenser head 164 around the periphery of the semiconductor die 450 so that the dielectric filler material 166 flows under the semiconductor die 450 and around the conductive bumps 456 adjacent the die periphery. As such, the dielectric filler material 166 is only needed proximate the conductive bumps 456 and not under the entire die as done conventionally. The semiconductor die 450 may be left exposed or encapsulated by encapsulation apparatus 178, which may provide encapsulation material 168 to the semiconductor assembly 460 via dispensing, spin-coating, glob-topping, depositing, transfer molding, or any other suitable method known in the art. It is preferred that such encapsulation material 168 be applied to the back side or surface 454 of the semiconductor die 450 at the wafer level or prior to dispensing

the dielectric filler material 166 about the periphery to facilitate fully encapsulating the semiconductor die 450.

Please amend paragraph **[00102]** as follows:

[00102] As a further approach to implementing the present invention, and as depicted in FIG. 29, an interposer substrate 110 may be provided having conductive traces 124 laminated thereto, the bottoms thereof being fully covered or, optionally, uncovered by solder mask 118, and a conductive bump 156a formed by reflow (if solder) or curing (if an epoxy) of a mass of conductive paste 182 at the bottom of each recess 120. A dielectric filler material 166 is then disposed over conductive bumps 156a in each recess 120 as shown. A semiconductor die 150 carrying a like plurality of conductive bumps 156b arranged for superimposed contact with conductive bumps 156a when semiconductor die 150 is aligned with interposer substrate 110 is then aligned over interposer substrate 110 and vertically pressed thereagainst as depicted by arrow M, the semiconductor die 150 placement motion squeezing the nondielectric filler material laterally outward so that conductive bumps 156a and 156b meet and make conductive contact. Adhesive elements 116 may, as shown, be used, or may be omitted, as desired.

Please amend paragraph **[00103]** as follows:

[00103] In a variation of the approach of FIG. 29, it is also contemplated that, in lieu of using dielectric filler material 166 and to provide an interposer substrate-to-die adhesive instead of using a separate adhesive element 116, a nonconductive film NCF, as shown in broken lines in FIG. 29 may be disposed over interposer substrate 110 after formation of conductive bumps 156a thereon and prior to assembly with a semiconductor die 150 carrying conductive bumps 156b. When the semiconductor die 150 and interposer substrate 110 are pressed together, conductive bumps 156a and 156b will penetrate the nonconductive film to initiate mutual electrical contact therebetween. Suitable nonconductive films include the UF511 and UF527 films offered by Hitachi Chemical Co., Ltd., Semiconductor Material Division, Japan.